The new G3RUH software modem for the DSP56002EVM

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Abstract

This paper presents the new design of the G3RUH software modem. This is a two level PAM modem that works at range of bit rates from 9600bps to 38400bps and admits different rates at transmission and reception. The major improvement of this new version is the synchronism algorithm and the structure of the reception filter. It provides a better performance of the modem. The software is aimed for the DSP56002EVM from Motorola as this is one of the most extended platforms in the ham radio.

1. Introduction

In 1999 our research group developed a software G3RUH modem for the DSP56002EVM compatible with the hardware G3RUH [1] at the rates of 9600, 19200, 28800 or 38400bps based on the software version of the 9600bps modem developed by Jarkko Vuori [2]. Our version permitted the selection of different rates in transmission and reception, but presented some problems when running at 38400bps mainly due to lost of synchronism.

The new version presented in this paper gets a better performance by consequence of the new synchronism algorithm and the polyphase structure of the reception filter.

2. Functional structure

The structure of this modem, which is shown in Figure 1, matches with the general one of a base-band modem.

The modulator consists of the first two blocks: the scrambler and the transmission filter. The next block represents the channel, which is supposed to be flat and noise additive. The rest of the blocks develop demodulation, by means of the reception filter, the AGC, the threshold detector, the synchronism recovery subsystem, the unscrambler and the DCD.

In the following sections the implementation of each block is described, with emphasis on the transmission and reception filters and the synchronism details.

3. Scrambler - Unscrambler

The scrambler aleatorizes the data to be sent providing a flatter spectrum in transmission. It also makes the synchronism process easier and reduces the DC component. The unscrambler restores the original data from the received data.

Scrambler and unscrambler are self-synchronizing and employ the same polynomial as the hardware version to provide compatibility [1].

4. AGC

The Automatic Gain Control attempts to maintain a constant signal level before decision. As the codec gain of the DSP56002EVM cannot be changed while running, this block acts on the sampled signal.

The algorithm searches for the biggest value of the signal within a group of samples and adjusts the gain value in accordance.

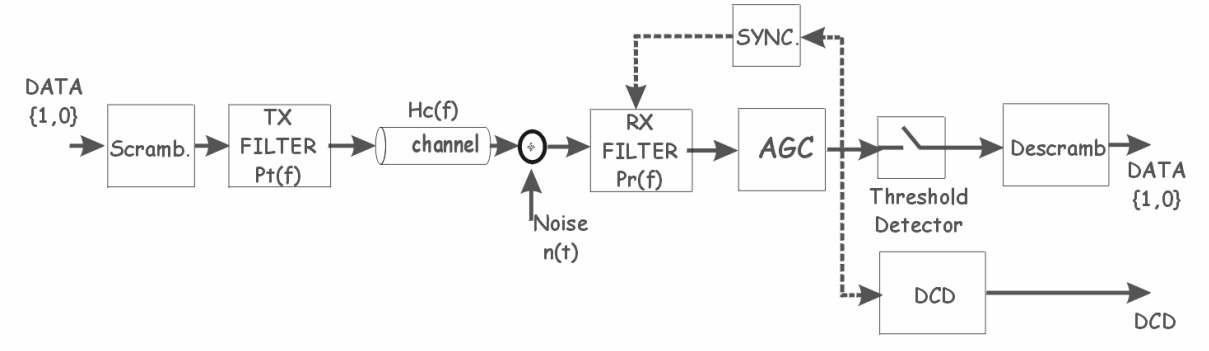

Figure 1. Functional structure of the G3RUH modem

5. DCD

The Data Carrier Detect block validates the received data. It uses the Eye's Aperture to decide if there is any incoming data. When the Eye's Aperture is bigger than a certain threshold, the received data is valid [2].

6. Tx and Rx Filters

The filters were designed considering the Nyquist criterion to minimize the effect of ISI and the matched filter criterion to maximize the received SNR. The result is a set of two square root raised cosine filters, one for transmission and another one for reception. The selected roll-off factor is the same as the first software version of [2].

The bandwidth of the raised cosine filters depends on the selected bit rate and the roll-off factor. Table 1 shows the necessary bandwidth at each rate.

BIT RATE	ROLL-OFF FACTOR	SIGNAL BANDWIDTH
9K6	0.3	6,440 Hz
19K2	0.3	12,480 Hz
28K8	0.3	18,720 Hz
38K4	0.3	24,960 Hz
38K4	0.2	23,040 Hz

Table 1. Necessary bandwidth as a function of the bit rate and roll-off factor.

The codec of the DSP56002EVM has a maximum sample rate of 48,000 samples/s, so the maximum bandwidth of the analog input signal is 24,000 Hz. Table 1 shows that at a bit rate of 38,400bps, with a roll-off factor of 0.3, the necessary bandwidth (24,960Hz) is greater than the available bandwidth (24,000Hz). To solve this problem, the roll-off factor is reduced to 0.2.

This change of the roll-off value will produce a reduction on the performance of the modem when working against a hardware version.

6.1. Transmission filter

The transmission filter is designed using a polyphase structure due to its multirate character.

The codec will be working at 48,000 samples per second, so the output of the filter should provide that rate of samples to the codec at all the modem rates. To achieve this, the structure shown in Figure 2 is used.

The system performs zero padding, filtering and decimation. The zero padding process, increases the working rate of the filter, leading to the figures shown in Table 2. The decimator converts the filter sample rate to the 48,000 samples per second required by the codec. Some samples will be thus ignored, and will not be calculated. This process is known as multirate filtering [3] [4].

BIT RATE	FILTER SAMPLE RATE	DECIMA-TION FACTOR	POLYPHASE SEQUENCE
9K6	48,000	1	0 1 2 3 4
19K2	96,000	2	0 2 4 1 3
28K8	144,000	3	0 3 1 4 2
38K4	192,000	4	0 4 3 2 1

Table 2. Characteristics of the transmission filter.

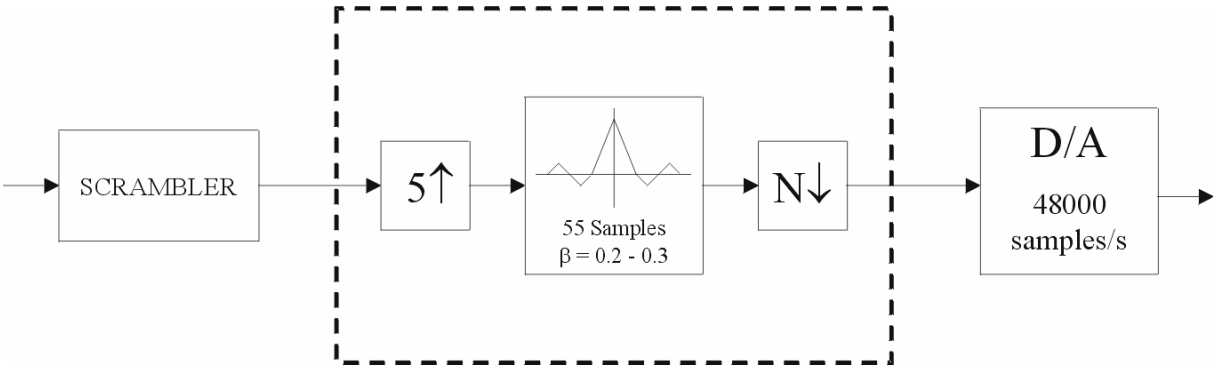

Figure 2. Structure of the transmission filter.

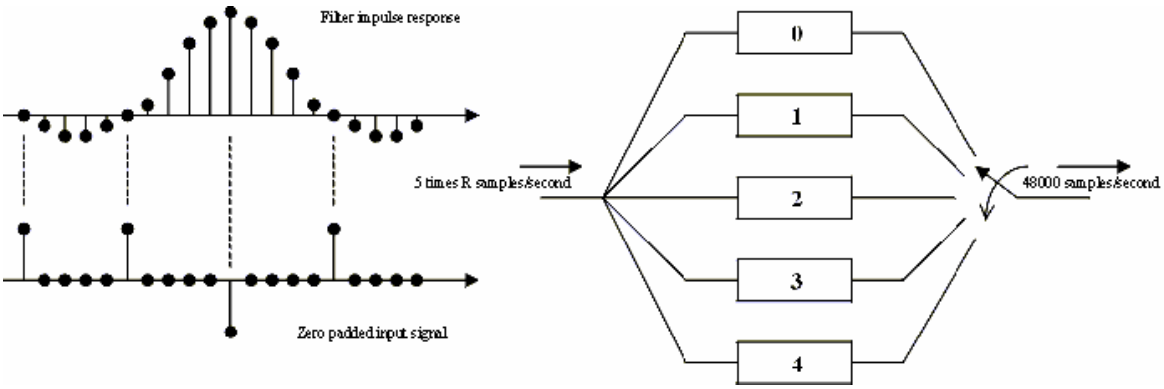

Figure 3. Multirate processing

Figure 3 shows the multirate processing system. The filter length would be 55 samples. At the input of the filter we will find four zeros between the two data bits. If we used this zero padded sequence in the filtering process, a high number of multiplications by zero would take place. To avoid this, the filter is divided into five subfilters, called *polyphase* filters, numbered from 0 to 4 in Figure 3. Each *polyphase* includes the 11 coefficients of the filter that would not be multiplicated by a padded zero input sample.

As only the samples required by the codec are calculated, a different sequence of polyphases is used at every rate and the step in the sequence is given by the decimation factor. In this way, at the rate of 9600bps 5 samples/bit are necessary, so we must use one output sample from each polyphase filter. At the 19200bps rate we need five samples every two bits, so we will use the output of the 0, 2, and 4 polyphases for the first bit and 1, 3 for a second bit. The sequence of polyphases used for every rate is shown in Table 2.

6.2. Reception filter

In order to perform detection the optimum decision time instant must be calculated, and the more time resolution is available, the better. Thus, a high number of samples per bit should be available. In our design the demodulator can calculate up to 80 samples per bit period. However, we only need two samples to perform synchronism recovery and the detection, so just two out of 80 will actually be calculated, avoiding computing overhead.

To perform this sample rate conversion we use the same multirate filtering structure for the reception filter as the one used in transmission, now with a constant decimation factor of 40 to downsample from 80 to two. The reception filter architecture is shown in Figure 4. The filter used with a roll-off factor of 0.3 is 768 samples long, and 576 for 0.2.

The interpolation factor depends on the bit rate and sets the number of coefficients of each polyphase filter. Table 4 shows the figures. At every bit rate, the interpolation factor is such that converts from 48000samples per second to 80 times the bit rate.

BIT RATE	INTERPOLATION FACTOR	COEFFS PER POLYPHASE
9K6	16	36
19K2	32	18
28K8	48	12
38K4	64	12

Table 4. Parameters of the reception filter.

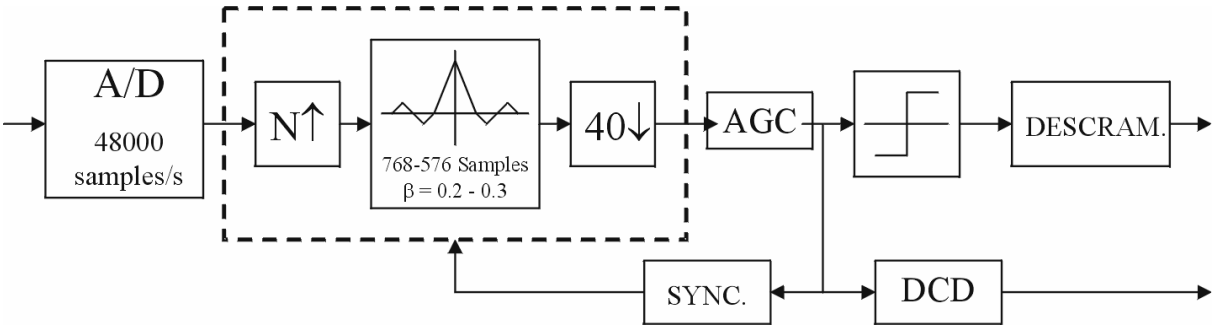

Figure 4. Structure of the reception filter.

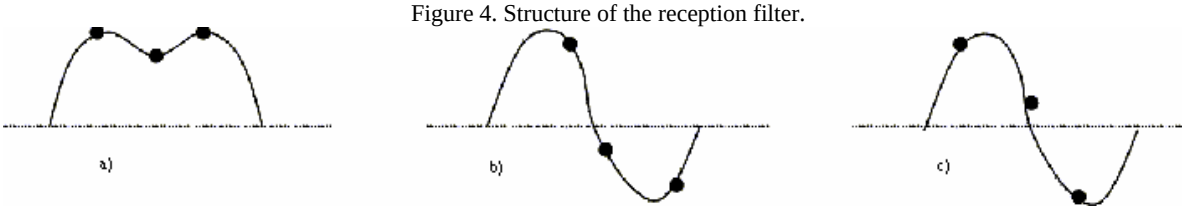

Figure 5. Possible locations of the samples in the synchronism recovery.

7. Synchronism recovery

The synchronism recovery algorithm uses the two samples corresponding to the center and the beginning of the bit symbol, and performs a comparison between their values. The three possible situations are shown in Figure 5. If a transition between bits has no zero crossing, the synchronism cannot operate (Figure 5a).

In case a transition occurs, we observed the value of the border sample. If it is located before the zero crossing, a variable is increased (Figure 5c). In the opposite situation, the same variable is decreased (Figure 5b).

For every received symbol, the synchronism algorithm tests the value of the variable to decide whether an adjustment in synchronism has to be done. When the variable's value is greater than a positive threshold or smaller than a negative one, an adjustment is perform by going up or down in the polyphase structure, selecting a new set of filters for the two samples to be calculated.

The up/down stepping is done with acceleration, with step values varying from one to eight. If the present necessary correction is in the same direction as the previous one, the step in the correction is duplicated, so as to reach more quickly the optimum state. If the present necessary correction is in the opposite direction or no correction has been performed during a certain number of consecutive symbols, the step value is divided by two, so as to refine the search of the optimum state.

8. Conclusions

A new software modem running a variable bit rates has been described here. This modem has proved a very good performance, even when it is use with a hardware version of the G3RUH modem at the highest bit rates.

Acknowledgments

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